DESIGN OPTIMIZATION OF MICROWAVE POWER HETEROJUNCTION BIPOLAR TRANSISTOR CELLS

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ABSTRACT

Results of a design optimization study of power heterojunction bipolar transistor cells are presented. AlGaAs/GaAs HBTs have been fabricated using a simple heterostructure design grown by molecular beam epitaxy and a novel self-aligned fabrication process which offers relatively low parasitics. The influence of power transistor cell design on device performance is emphasized. The design optimization study involved simultaneous fabrication of transistor cells with a relatively wide range of geometries. Transistors with a wide range of emitter finger sizes and number of emitter fingers, but with the same number of collector contacts and the same basic cell design approach, have been fabricated and characterized by DC and microwave testing. The results of this study provide a basis for obtaining further improvements in microwave power HBT performance.

INTRODUCTION

Heterojunction bipolar transistors (HBTs) are promising candidates for microwave power applications owing to their high power added efficiency. Recent work on AlGaAs/GaAs power HBTs has reported (1) 0.4 W cw power operation at 10 GHz with 48 % power added efficiency and 7 dB power gain. Power outputs as high as 1 W with 49 % efficiency and 6 dB gain have already been obtained (2) at 5 GHz. Other work (3) has demonstrated (pulsed operation at 10 GHz) that HBT power output scales with emitter periphery and number of transistor cells up to powers of 1 W while maintaining power added efficiency in the range of 40 - 50 %. These recent results show that HBTs are attractive candidates for further development for microwave power applications.

Due to the rapid experimental progress being achieved in HBT development, it is now important to undertake a design optimization study of HBTs for power microwave applications. In the present work, we report the analysis and device results of a design optimization study of AlGaAs/GaAs HBTs for power applications.

DEVICE DESIGN AND FABRICATION

The AlGaAs/GaAs HBTs were fabricated from molecular beam epitaxial (MBE) layers grown on 3 inch diameter semi-insulating GaAs substrates. The HBT epitaxial layer structure is shown in Table I. A simple seven-layer MBE-grown HBT structure was used as the baseline epitaxial layer design for this study. The HBT heterostructure consists of: an n^+ (2×10^{18} cm^{-3}) 0.25 um thick GaAs subcollector; an n (5×10^{17} cm^{-3}) 0.5 um thick GaAs collector; a p^+ (1×10^{19} cm^{-3}) GaAs base layer, an undoped 0.02 um thick spacer layer; an N (3×10^{17} cm^{-3}) $Al_{0.3}Ga_{0.7}As$ emitter; an n (3×10^{17} cm^{-3}) 0.04 um thick emitter cap graded layer with aluminum composition graded from 0 to 30 % in the emitter; and finally, an n^+ (4×10^{18} cm^{-3}) 0.25 um thick GaAs cap layer. This heterostructure design was not optimized for power operation, eg. high breakdown voltage, but was utilized as the baseline design to permit comparison of transistor cell layouts.

Table I. HBT Epitaxial Layer Structure

LAYER	THICKNESS (um)	TYPE	DOPING cm^{-3}	AlAs FRACTION
CAP	0.25	n^+	4×10^{18}	0
EMITTER CAP GRADE	0.04	N	3×10^{17}	0 - 0.3
EMITTER	0.04	N	3×10^{17}	0.3
SPACER	0.02	---	UNDOPED	0
BASE	0.1	p^+	1×10^{19}	0
COLLECTOR	0.5	n	5×10^{17}	0
SUBCOLLECTOR	0.25	n^+	2×10^{18}	0

+QQ801

In the present work, we focus on the effects of power transistor cell design on device performance. Clearly, parasitic resistances and capacitances which would compromise device performance must be minimized. To minimize parasitics, we employ a novel self-aligned fabrication approach which reduces the emitter-base and base-collector spacings. The HBT fabrication process also features the use of silicon nitride for passivation and to allow self-alignment of the collector contact.

Figure 1 shows a cross sectional schematic of the self-aligned HBT. Device fabrication begins with the isolation step which is performed using hydrogen and fluorine ion implantation. After AuGe/Ni/Au emitter ohmic metal deposition and lift-off, the emitter layer is chemically etched to reveal the base layer. The Au/Zn/Au p-type base contact is then deposited using the emitter metal as the self-alignment mask. PECVD silicon nitride is used to mask the emitter-base area during the collector etch. Collector contacts are aligned to both ends of the emitter-base active area. After AuGe/Ni/Au collector ohmic metal deposition, the emitter, base, and collector contacts are alloyed simultaneously on a hot plate. Interconnect is completed by forming 3-um high electroplated gold airbridges.

The design optimization study described here involved simultaneous fabrication of transistor cells with a relatively wide range of geometries utilizing the above fabrication process. While retaining the same number of collector contacts, transistors with a wide range of emitter finger sizes (finger sizes from 1x5 to 1x20 um^2) and number of emitter fingers (from 2 to 10 fingers) were fabricated and tested. These transistors with different emitter designs are to be used as the unit cell in multi-cell power transistors. An SEM microphotograph

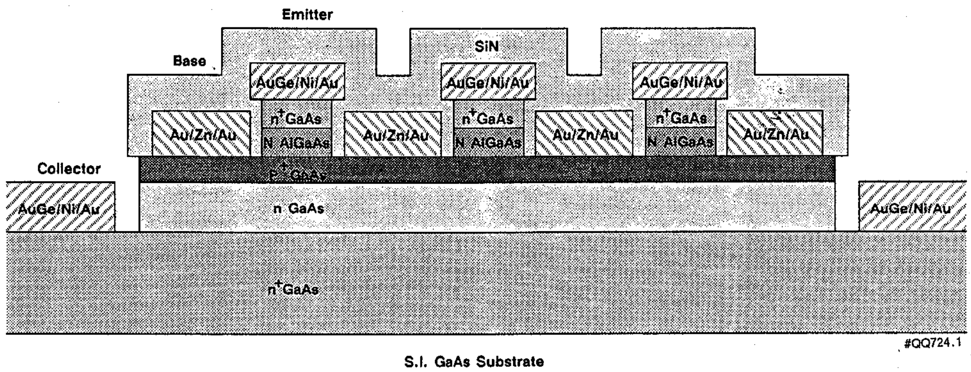

Fig. 1. A cross sectional schematic of the self-aligned HBT with 3 emitter fingers.

of a representative HBT with ten 1x10 um^2 fingers is shown in Fig. 2.

DC AND MICROWAVE DEVICE PERFORMANCE

Figure 3 shows typical I-V characteristics of the HBT with two 1x5 um^2 emitter fingers. This HBT is the smallest device in our study. As shown in Fig. 4, this device with two 1x5 um^2 fingers exhibits a typical beta of 14 and a maximum emitter current density of 1 x 10^5 A/cm^2. Results of the S-parameter measurements performed with an HP8510 network analyzer and microwave probes are shown in Figs. 5 and 6. For the data of Figs. 5 and 6, the bias point is set at V_{CE} = 2.4 V and I_C = 4.5 mA. The device is biased to operate near the center of the device operating range so as to be representative of typical device performance. The Maximum Available Gain (MAG) and Current Gain as a function of frequency were calculated from the S-parameters and are shown in Fig. 6. The MAG cut-off frequency (f_{MAG}) for this device with two 1x5 um^2 emitter fingers was measured to be 23.8 GHz and the current-gain cut-off frequency (f_T) was extrapolated to be 31.2 GHz using a -6 dB/octave slope.

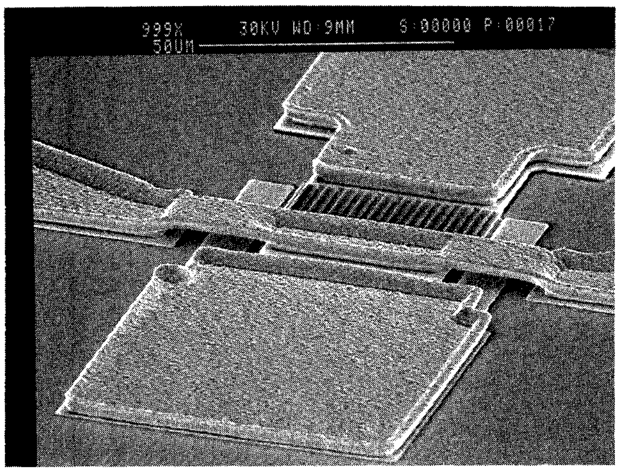

Fig. 2. An SEM microphotograph of the self-aligned HBT with ten 1x10 um^2 emitter fingers.

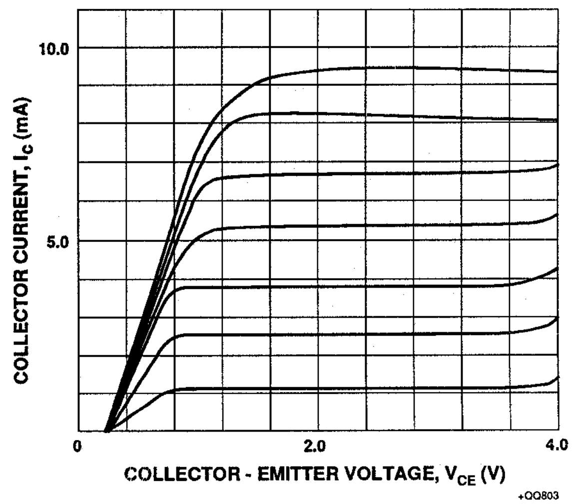

Fig. 3. Typical collector I-V characteristics of the HBT with two 1x5 um^2 emitter fingers.

The DC performance as a function of emitter finger length is shown in Fig. 7. As the emitter finger size of the two finger device is increased from 1x5 um^2 to 1x10 um^2 and 1x20 um^2, beta increases slightly and the maximum current density increases with increasing emitter finger area. However, the high frequency performance shown in Fig. 8 suffers moderately as f_T degrades by 3 GHz (10%) for the 1x10 um^2 finger and 8 GHz (26%) for the 1x20 um^2 finger as compared to the 1x5 um^2 finger device. The f_{MAG} also degrades by 2 GHz (8%) and 6 GHz (25%) for 1x10 um^2 and 1x20 um^2 devices, respectively.

The power performance of the HBT is determined by the breakdown voltage and the current capability of the transistor. The HBT breakdown voltage is determined largely by the epitaxial layer structure. The current, and hence HBT power performance, can be improved by increasing the emitter finger area while assuring that the design offers acceptable high frequency performance. Severe limitations on the high frequency performance

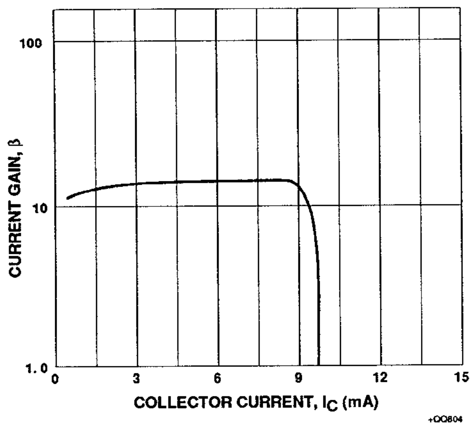

Fig. 4. Current gain as a function of collector current showing the maximum current of the HBT with two 1x5 um² emitter fingers. The maximum collector current for this device is ~9.5 mA with V_{CE} = 2.5 V.

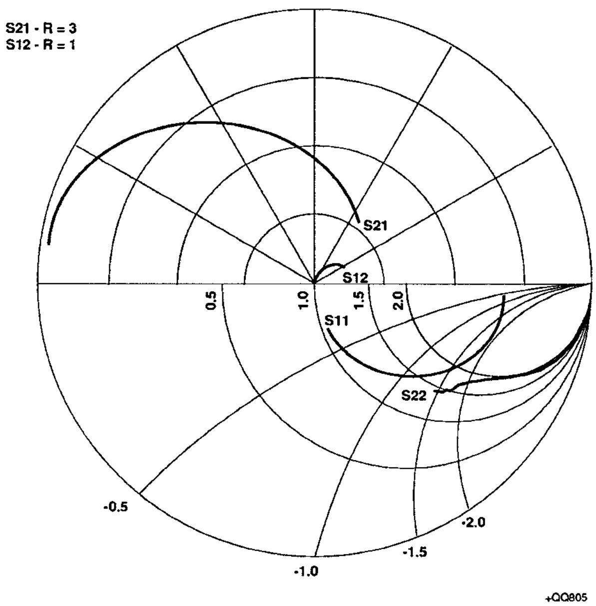

Fig. 5. Measured S-parameters of the self-aligned HBT biased at V_{CE} = 2.4 V and I_C= 4.5 mA.

and maximum current density of our design are imposed by the number of emitter fingers. Figure 9 shows the high frequencv performance as a function of the number of 1x10 um² emitter fingers. As the number of 1x10 um² fingers increases from 2 to 5, an increase of the effective emitter area by 250%, f_T and f_{MAG} degrade by 14 GHz (50%) and 9 GHz (41%), respectively. This drastic degradation of the HBT high frequency performance is due to the increase in both the collector resistance and collector-base junction capacitance. The maximum current density also degrades rapidly as the number of emitter fingers increases as shown in Fig. 10. The maximum current density decreases by 54% as the number of fingers increases from 2 to 5. We find that increasing the number of emitter fingers beyond three in our transistor cell design does not increase the maximum

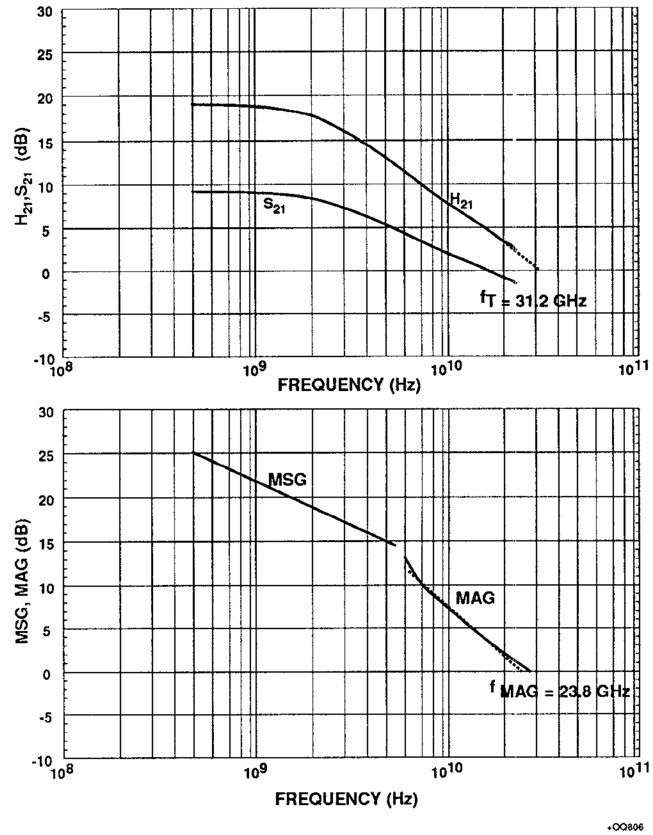

Fig. 6. Maximum available gain (MAG) and current gain versus frequency for the HBT with two 1x5 um² emitter fingers. The current gain cut-off frequency, f_T, and the MAG cut-off frequency, f_{MAG}, are 31.2 GHz and 23.8 GHz, respectively.

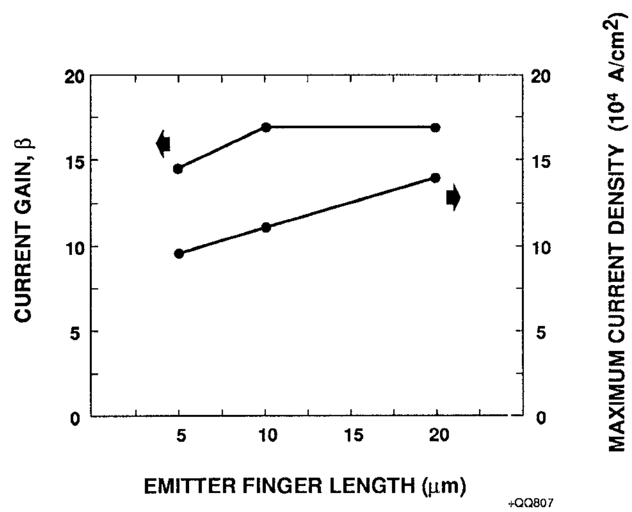

Fig. 7. HBT DC current gain and maximum current density as a function of emitter finger length.

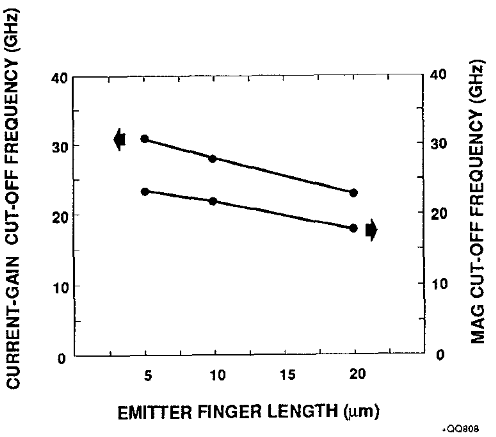

Fig. 8. The HBT current gain cut-off frequency, f_T, and MAG cut-off frequency, f_{MAG} as a function of emitter finger length.

current substantially because of the resulting excess collector resistance.

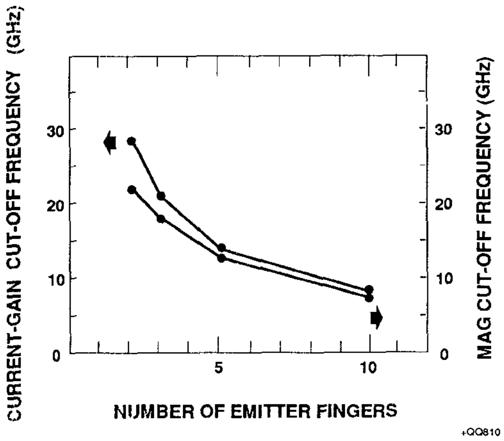

Fig. 9. The HBT current gain cut-off frequency, f_T, and MAG cut-off frequency, f_{MAG}, versus number of emitter fingers. The emitter finger size is 1x10 um^2

SUMMARY AND CONCLUSIONS

In summary, we have reported the results of a design optimization study of heterojunction bipolar transistors for power microwave applications. AlGaAs HBTs have been designed and fabricated using a simple MBE heterostructure and a novel self-aligned fabrication process. The study has centered on the effects of power transistor cell design on device performance. We have fabricated and characterized HBTs with a relatively wide range of emitter finger sizes and number of emitter fingers. The DC test results indicate that the HBTs with more than three fingers do not exhibit a higher maximum current in spite of the additional emitter area due to high parasitic collector resistance and the resultant current crowding. Moreover, the microwave test results show that adding emitter fingers in our design merely increases the parasitic base-collector capacitance and drastically

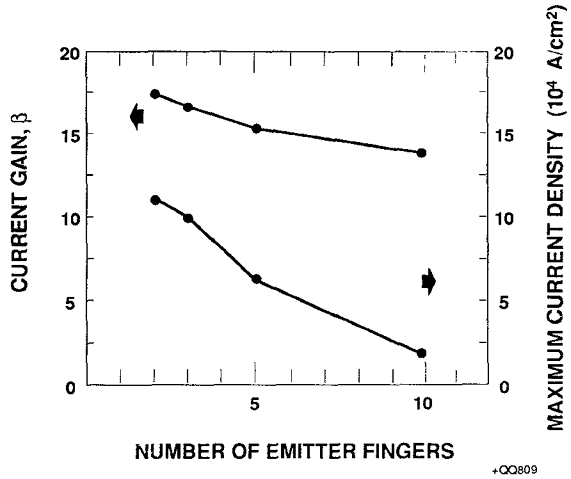

Fig. 10. HBT DC current gain and maximum current density versus number of emitter fingers. The emitter finger size is 1x10 um^2.

reduces f_T and f_{MAG}. In contrast, using a smaller number of longer emitter fingers yields devices with highest maximum current density while maintaining acceptable high frequency performance. In general, emitter finger lengths may be limited by emitter resistance and, finally, phase matching considerations. Further improvement in the performance of these devices can be obtained by reducing the collector resistance and the base-collector capacitance. The base-collector capacitance can be reduced by using an isolating implant of the extrinsic base area beneath the base ohmic contact (4). The collector resistance can be reduced by providing a transistor cell design which incorporates an interdigitated collector contact in a multi-cell power transistor. The results presented here provide a basis for obtaining further improvements in microwave power HBT performance.

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